



SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling

By *Stuart Sutherland, Simon Davidmann, Peter Flake*

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In its updated second edition, this book has been extensively revised on a chapter by chapter basis. The book accurately reflects the syntax and semantic changes to the SystemVerilog language standard, making it an essential reference for systems professionals who need the latest version information. In addition, the second edition features a new chapter explaining the SystemVerilog "packages", a new appendix that summarizes the synthesis guidelines presented throughout the book, and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys, Mentor, and Cadence tools.

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Editorial Review

From the Back Cover

SystemVerilog is a rich set of extensions to the Verilog Hardware Description Language (Verilog HDL). SystemVerilog for Design describes the correct usage of these extensions for modeling digital designs. These important extensions enable the representation of complex digital logic in concise, accurate, and reusable hardware models. All key SystemVerilog design features are presented, such as declaration spaces, two-state data types, enumerated types, user-defined types, structures, unions, interfaces, and RTL coding extensions. Emphasis is placed on the proper usage of these enhancements for simulation and synthesis. Design engineers, engineering managers and engineering students working with all sizes and types of digital designs, whether FPGA, ASIC or full custom, will find this book to be an invaluable learning tool and reference guide.

The second edition of this book reflects the official IEEE 1800-2005 SystemVerilog standard. This IEEE SystemVerilog standard adds new capabilities, clarifications, and changes to the Accellera 3.1 SystemVerilog upon which the first edition of this book was based.

Significant updates and revisions in the new edition include:

A new chapter showing how to use SystemVerilog packages with single-file and multi-file compilers.

- New code examples illustrating correct usage of the IEEE version of SystemVerilog.
- Updated coding guidelines reflecting the capabilities of current simulator and synthesis Electronic Design Automation tools such as digital simulators and synthesis compilers.

"SystemVerilog makes it easier to produce more efficient and concise descriptions of complex hardware designs. The authors of this book have been involved with the development of the language from the beginning, and who is better to learn from than those involved from day one?"

? Greg Spirakis, Vice President of Design Technology

Intel Corporation

"Sun has been a driving force in SystemVerilog from its inception. SystemVerilog can significantly improve the productivity of designers in the coming years, and this book is a comprehensive reference text for engineers who want to learn about SystemVerilog for their next generation designs."

? Sunil Joshi, Vice President of Software Technologies & Compute Resources

Sun Microsystems, Inc.

"SystemVerilog addresses the need for efficient and powerful modeling essential to support the complexity, size and scale of next generation hardware designs. This book explains how to use SystemVerilog effectively and provides numerous examples to illustrate how each of the language constructs can best be utilized."

? Chris Malachowsky, Co-Founder and Vice President of Hardware

NVIDIA Corp.

Users Review

From reader reviews:

Linda Gaitan:

Reading can called mind hangout, why? Because if you are reading a book especially book entitled SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling your brain will drift away trough every dimension, wandering in every single aspect that maybe unknown for but surely can become your mind friends. Imaging each and every word written in a publication then become one web form conclusion and explanation this maybe you never get before. The SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling giving you yet another experience more than blown away the mind but also giving you useful details for your better life in this era. So now let us demonstrate the relaxing pattern here is your body and mind will be pleased when you are finished studying it, like winning a game. Do you want to try this extraordinary wasting spare time activity?

Mary Salas:

Do you have something that that suits you such as book? The guide lovers usually prefer to choose book like comic, brief story and the biggest an example may be novel. Now, why not trying SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling that give your entertainment preference will be satisfied by means of reading this book. Reading behavior all over the world can be said as the opportunity for people to know world a great deal better then how they react towards the world. It can't be mentioned constantly that reading habit only for the geeky particular person but for all of you who wants to end up being success person. So , for every you who want to start looking at as your good habit, you are able to pick SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling become your own personal starter.

Arthur Haynes:

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